Performance Evaluation & Comparative Study of Dual Input non isolated DC-DC Converters for Hybrid Power Systems

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Abstract: Traditionally hybrid power generation systems involving same or different renewable sources as input sources AC coupled or DC coupled to the load requires an individual power electronic converter stage for each source. This type of topology needs individual controller for regulating the output voltage. This limitation can be overcome by developing multi input converters which are capable of delivering power to the load individually or simultaneously to the load. Also this methodology would require one controller for managing the power flow effectively and economically. In this paper an attempt is made to evaluate the performance parameters viz efficiency , voltage regulation and ripple in the voltage and current for different topologies of Dual input DC-DC converters which are synthesized as per definite rules and guidelines and compared. Each of the topology is designed for a fixed load and simulated in MATLAB SIMULINK platform to evaluate the performance parameters. For getting better efficiency, less voltage ripple, and less current ripple for different converters with constant output voltage by varying duty ratios. From the results comparison SEPIC topology is evident that is most suitable topology.

Keywords: Dual Input converters (DIC) , DC distribution systems, microgrid,Pulsating voltage source cell (PVSC), Pulsating current source cell(PCSC) , Multi Input Converter(MIC).

Introduction

DC distribution systems are applied mostly in communications systems, data centers, and micro grids. The development of a distributed generation system with the usage of renewable energy sources like solar energy, wind energy is the only solution to overcome the limitations of power generation using fossil fuels. But the biggest disadvantage of using these resources independtly is their intermittent nature that makes the system very unreliable. To overcome this disadvantage hybrid power systems can be developed with different sources which has the ability to transfer energy to the load individually or simultaneously. The hybrid power generation system with the number of renewable energy sources connected to a common load requires as many DC-DC converters as number of sources, and such configurations require individual controller to regulate the output voltage. This system require number of single input converters depending on the number of sources which leads to the complexity in the structure as well as in control. Instead, the use of multi input DC-DC Converters have several advantages as it can contain lesser passive equipments and a single controller to control many converters. Hence, Dual Input converters are used to combine the local power sources into a dc power distribution architecture forming a micro grid with the ability of power flow independently or collectively.[1][2]

It is very important to derive multi input converters from single input converters. Many MIC topologies have been proposed in literature to integrate multiple sources to achieve cost effectiness and to reduce the complexity of the system. In this regard there are many isolated and non isolated topologies proposed in th literature. Several assumptions, restrictions, and conditions for identifying the feasible topologies of MICs are discussed in [3] which are realized from their single-input converters. A systematic approach for synthesizing different DIC topologies is basically derived from the six basic non isolated converters such as buck, boost, buck–boost, Cuk, Zeta, and SEPIC converters. [4]-[7].The topologies discussed (3)-(5) can be classified into two types depending on whether source and load are isolated or not.

This paper aims at the validation of the working of various non isolated topologies and to exhibit required performance of maintaining the constant output voltage through simulations. The performance parameters are being compared for the selection of a suitable topology for hybrid power generation with renewable sources as inputs.

This paper is organized as follows section II gives brief description of synthesis procedure of MIC section III gives the validation of MIC's using MATLAB simulink tool and section IV gives tabulated results of MICs with variation in input. Section V gives conclusion.

Fundamentals of Synthesizing MICs

Basically synthesis involves decomposition of PWM converters into basic building cells such as pulsating voltage source cell (PVSC) or pulsating current source cells (PCSC) and output filter (LC or C) With set of rules, assumptions and guidelines. The MICs can be derived by adding the PVSCs or the PCSCs into the basic PWM converters. A PVSC or PCSC is inserted into the PWM converter that forms another PWM converter which termed as pulsating-source-derived (PS-derived) converter. Generally two families of MIC topologies can be generated one which can transfer power simultaneously or individually. Another one which can transfer power one at a time. Different PWM converters can be put in series to implement MIC. It continues to operate even if one of the sources has failed. Another way is to put the PWM converter in parallel with or with out electrical isolation. But this would not result in minimization of passive components. The control scheme with the parallel DC sources are based on time multiplexing concept so power transfer can not happen simultaneously. To address all these issues a systematic approach to synthesize MIC was proposed with certain assumptions, rules and guidelines. The resultant MIC should be capable of delivering power simultaneously when all sources are active or should transfer power with one source active and no power is transferred from one source to other. Systematic synthesis of MIC can reduce the number of inductors and capacitors as compared to simply paralleling the outputs of the converters and gives higher converter utilization.

A basic PVSC provides high frequency pulsating voltage source consist ov voltage source and switch network, basically three types of PVSC's are identified

Class A : DC voltage source is independent voltage source Ex: Buck

Class B; DC voltage source is intermediate storage voltage Ex: Cuk

Class 3: DC voltage source is sum of input voltage source and intermediate storage voltage source.

A basic PCSC provides high frequency pulsating current cell consists of current source with a switch network. Basically ther are three classes of PCSC's

Class A: The dc current source is independent source. Ex: Boost

Class B; The dc current source is an intermediate storage current source Ex; Buck Boost

Class C: The dc current source is sum of both independent current source and intermediate source Ex.SEPIC

To synthesize a MIC using PVSC, as told earlier there are various PVSCs each of them can be connected in series with itself or other PVSC's ie buck-buck, buck-cuk,buck-zeta etc... Similarly To synthesise a MIC using PCSC, various PCSC can be connected in parallel with itself or other PCSC's ie Boost-Boost, Boost-Buck Boost, Boost-SEPIC etc.,

MIC's generated from classs B and Class C have added advantage in the choice of voltage conversion ratio so that the output voltage is lower than or higher than input voltages.

General Procedure:

1. Choose one of the basic PVSC or PCSC
2. Select one of the basic PWM converter that contain the current sink or current buffer, voltage sink or voltage buffer
3. Insert chosen PVSC or PCSC into the proper location ie the energy buffer portion and the output portion are the two feasible locations.
4. With a energy buffer or output a PVSC should be connected in series where as a PCSC should be connected in parallel.

When PVSC's or PCSC's are introduced into output portions of prime PWM converter the derived converter will have the feature of transferring power simultaneously or individually. But when introduced into the energy portion of prime PWM converter not all derived converter can be identified as MIC but then called as quassi MIC which lacks the property of transferring power individually.

Validation of Dual Input Converters

In order to reduce the system complexity and cost effectiveness, DICs are derived from the six basics non-isolated DC-DC converters such as buck, boost, buck-boost, Cuk, SEPIC and Zeta converters.

Synthesis of DIC is obtained by inserting PVSC or a PCSC into prime PWM converter. Two different input voltage sources can be fed to the common load through common LC or C filter. This paper focus at the validation of feasible DIC's and performance comparison of the converters. Each topology is designed with the following specifications

V_1=20-30V, V_2=15-25V, Power=100watt, Vo=40V. The designed values for the passive components are L_1=L_2=10mH,Co=10uf, Ro= 10ohm, Ls1=Ls2=10mH, Cb1=Cb2=10uF and switching frequency Fs= 100KHz. To maintain

the output voltage constant with the variation in input values of the two sources the duty ratios of the devices are adjusted appropriately. The efficiency, output voltage and ripple current are tabulated.

DI-Buck type with different converters

Figure 1 shows the Combining Buck PVSC with other prime converter. All the circuits are simulated and at different input voltages adjusting the duty cycle to get constant output voltage and respective efficiency is noted and is tabulate in tables 1.The variation of efficiency with the duty cycles are as shown in fig 2 and fig 3.

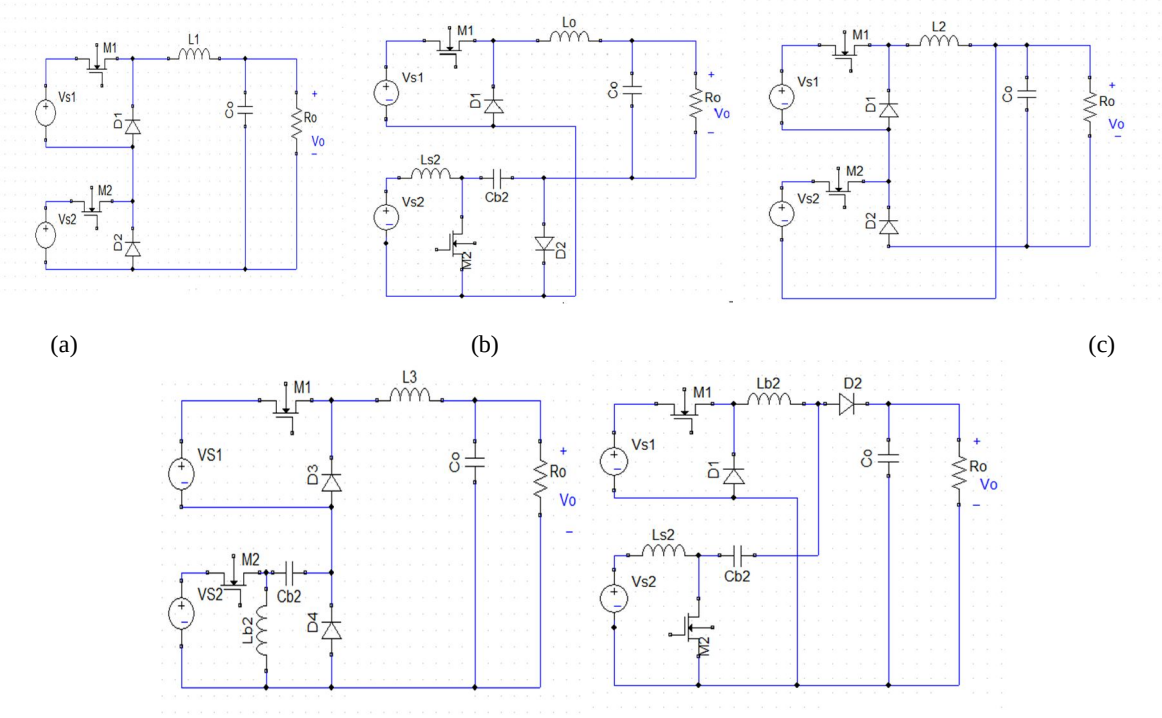


Fig 1:. (a) Buck-Buck converter. (b) Buck-Buckboost converter. (c) Buck-C´uk converter. (d) Buck-Zeta converter. (e) Buck-SEPIC converter

Table 1: Efficiency variation V/s Duty cycle D1 and D2

Duty Cycle		Efficiency				
D1	D2	BUCK-BUCK	BUCK-Boost	BUCK-CUK	BUCK-SEPIC	BUCK-ZETA
80	5	73.95	70.73	66.6	84.71	66.6
76	10	70.51	63.84	69.2	81.31	69.2
72	15	68.45	59.04	62.3	78.82	62.3
67.5	20	66.8	55.05	50.41	75.88	50.41
63.5	25	65.84	51.72	48.95	73.48	40.84
59	30	64.94	49.22	46.92	71.01	34.96
55	35	64.52	46.9	53.06	69.13	34.3
51	40	64.28	46.01	64.91	67.93	38.32
45	35	64.03	47.49	63	71.28	44.82

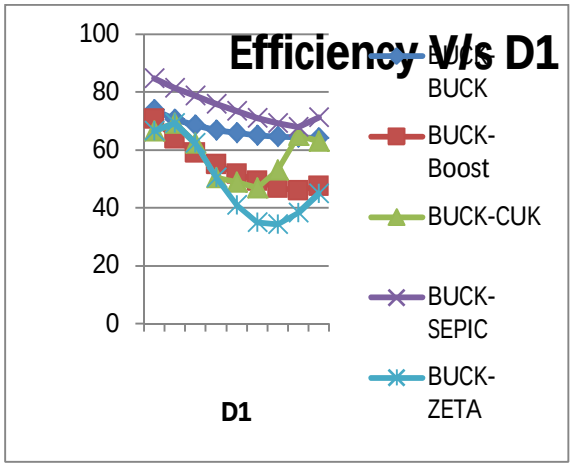


Fig 2: plot of efficiency with D1

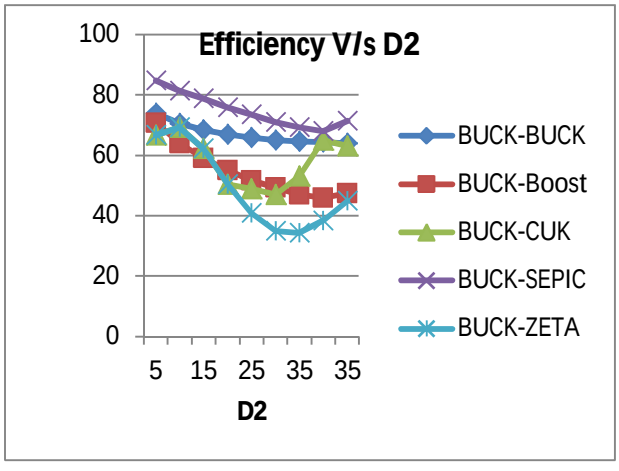
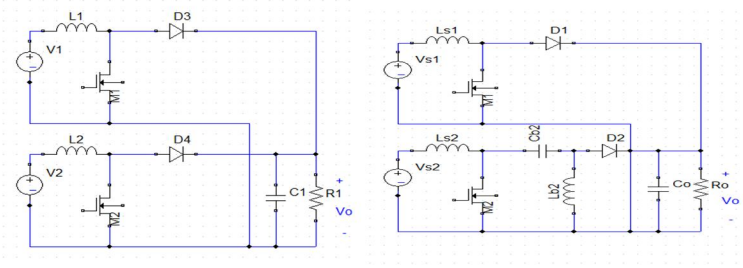


Fig 2: plot of efficiency with D2

DI-Boost type with different converters

Figure 4 shows the different DI-BOOST converter with other converters. Table 2 gives variation of efficiency with duty cycle D1 and D2. The respective plots are shown in Fig 5.



(a) (b)

Fig 4: (a) Boost-Boost converter. (b) Boost-SEPICconverter.

Table 2: Efficiency with D1 and D2

D1	D2	Boost-Boost	Boost-SEPIC
5	5	22.58	22.62
5	10	22.55	22.59
5	15	22.51	22.56
5	20	22.48	22.51
5	25	22.44	22.47
5	30	22.41	22.41
5	35	22.38	22.35
5	40	22.33	22.31
5	45	22.29	22.27

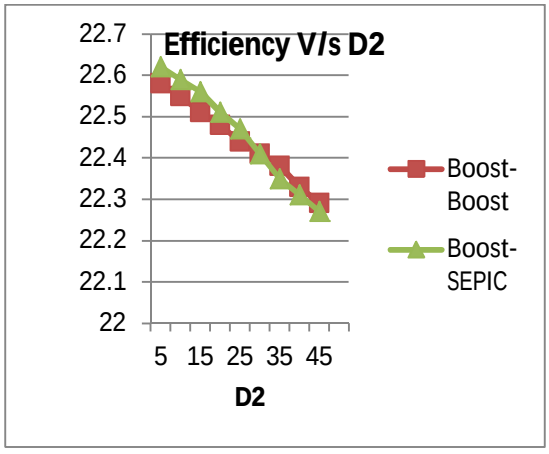
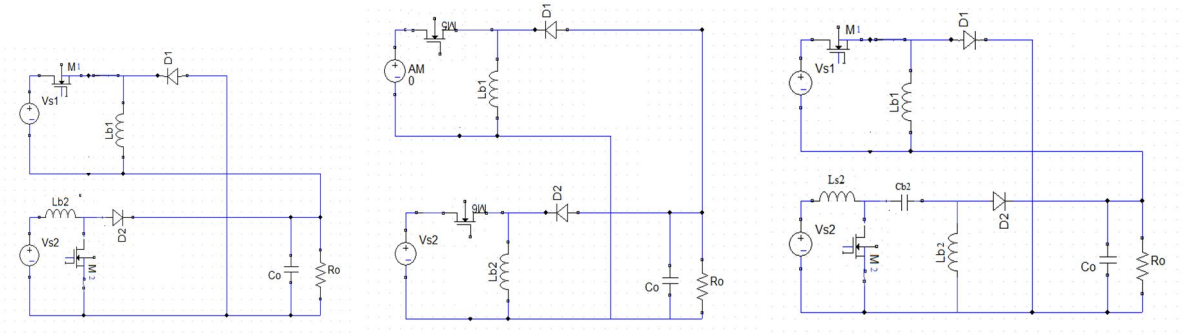


Fig 5: plot of efficiency with D2

DI-Buck-Boost type with different converters

Figure 6 shows the DI buck-boost converter. Table 3 gives variation of efficiency with duty cycle D1 and D2. The respective plots are shown in Fig 7.



(a) (b) (c)

Fig 6:. (a) BuckBoost-Boost converter. (b) BuckBoost -Buck–boost converter. (c) BuckBoost -SEPIC converter

Table 3: Variation of Efficency with D1 and D2

Duty Cycle		Efficiency	
D1	D2	Buck Boost-Buck	Buck Boost-SEPIC
45	5	57.63	57.75
45	10	57.41	57.43
45	15	57.19	56.98
45	20	56.91	56.75
45	25	56.56	56.49
45	30	57.52	46.26
45	35	57.29	56.14
45	40	57.06	57.61
45	45	56.76	57.22

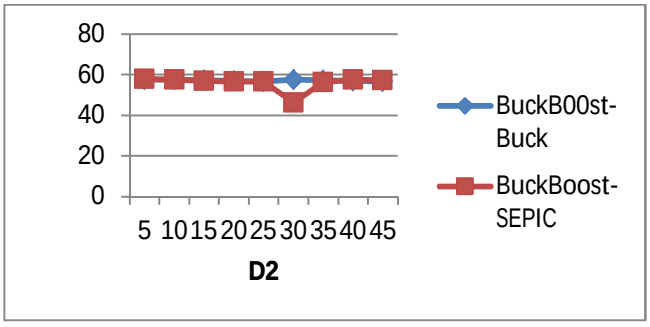


Fig 7: Plot of efficiency with D2

DI-C'uk type with different converters

Figure 8 shows the DI-C'uk converter. Table 4 gives variation of efficiency with duty cycle D1 and D2.The respective plots are shown in Fig 9 and Fig 10.

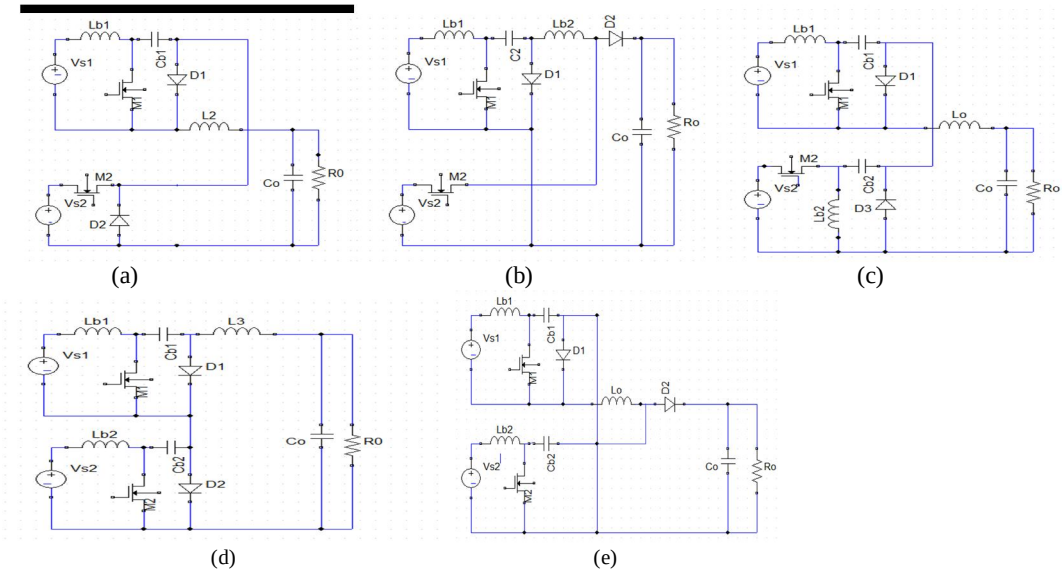


Fig 8: (a) Cuk-Buck converter. (b) Cuk- Buck–boost converter. (c) Cuk -C´uk converter. (d) Cuk -Zeta converter. (e) S Cuk - EPIC converter

Table 4: Efficiency with D1 & D2

Duty Cycle		Efficiency		
D1	D2	Cuk-Cuk	Cuk-BuckBoost	Suk-SEPIC
44.6	5	73.95	70.73	66.6
43.2	10	70.51	63.84	69.2
41.4	15	68.45	59.04	62.3
39.2	20	66.8	55.05	50.41
36.4	25	65.84	51.72	48.95
33	30	64.94	49.22	46.92
28.6	35	64.52	46.9	53.06
23	40	64.28	46.01	64.91
15	45	64.03	47.49	63

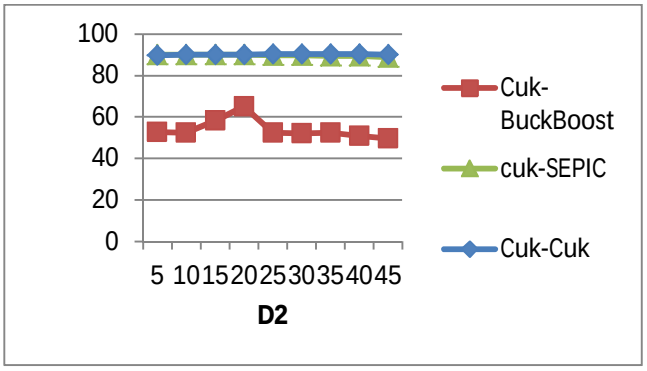


Fig 10: Plot of Efficiency with D1

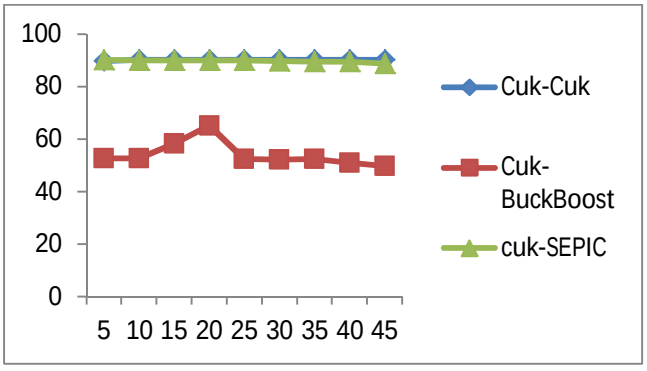
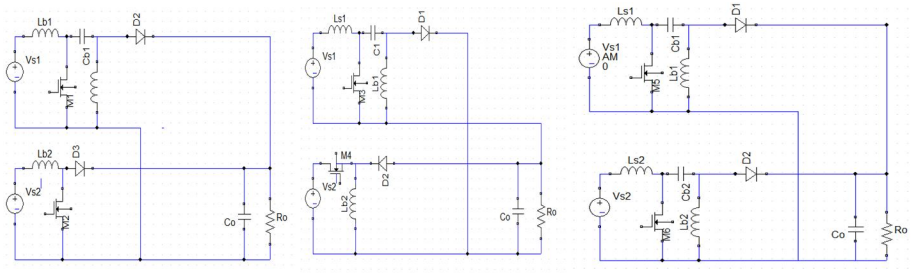


Fig 11: Plot of Efficiency with D2

SEPIC type with different converters

Figure 12 shows the DI-SEPIC converter. Table 5 gives variation of efficiency with D1 and D2. The respective plots are as shown in fig 13 and 1Fig 14.



a) (b) c)

Fig 12: (a) SEPIC-Boost converter. (b) SEPIC-Buck–boost converter. (c) SEPIC-SEPIC converter

Table 5: Variation of Efficiency V/s D1 and D2

SL NO	D1	D2	Efficiency
1	32	5	81.55
2	30	10	87.08
3	26	15	87.03
4	20	20	81.69
5	17	25	86.51
6	15	30	87.68
7	9	35	86.91
8	1	40	68.89

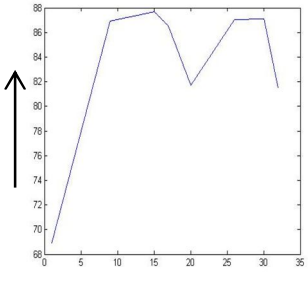


Fig 13: Efficiency vs D1

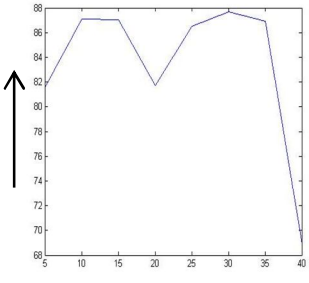


Fig 14: Efficiency vs D2

DI-Zeta type with different converters

Figure 14 shows the DI-Zeta converter. This converter is similar like SEPIC converter.

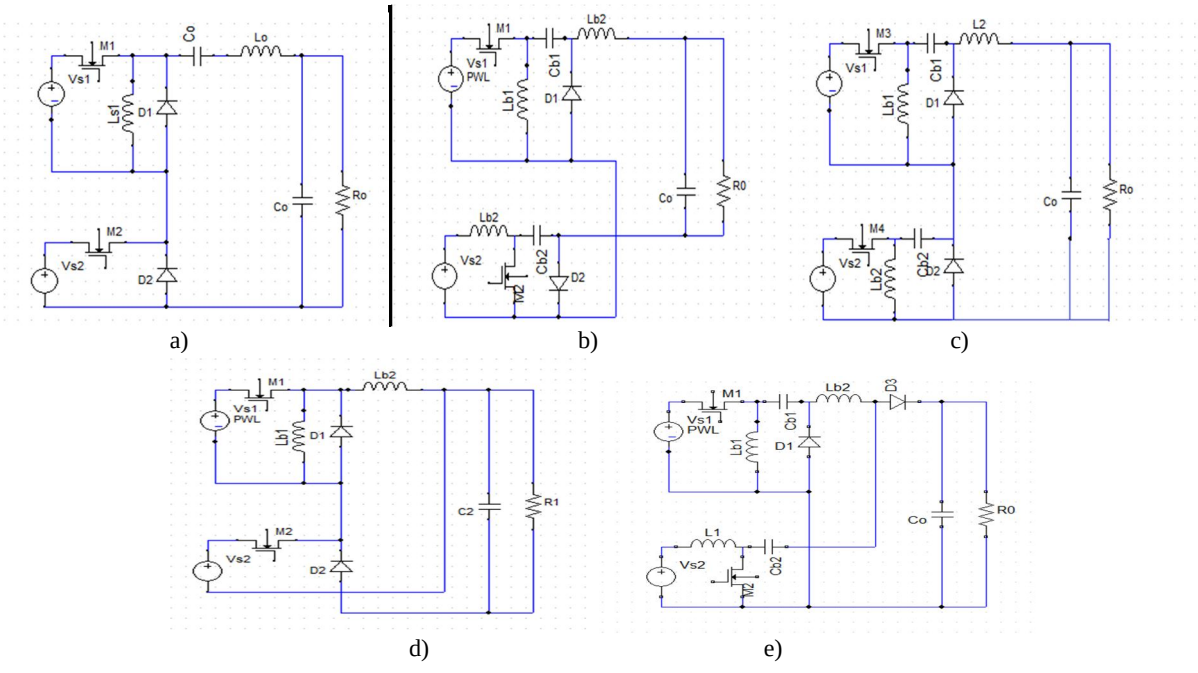


Fig 14: (a) ZETA-Buck converter. (b) ZETA-Buck–boost converter. (c) ZETA-C´ uk converter. (d) ZETA-Zeta converter. (e) ZETA-SEPIC converter

Table 6: Efficeny V/s D1 and D2

Duty Cycle		Efficiency		
D1	D2	ZETA-ZETA	ZETA-Buck Boost	ZETA-SEPIC
45	5	52.80	56.43	84.71
43.5	10	51.03	55.59	81.31
41.4	15	49.74	55.57	78.82
39.3	20	49.10	55.81	75.88
36.4	25	48.54	56.06	73.48
33	30	48.28	56.62	71.01
28.6	35	48.21	59.53	69.13
23	40	48.90	61.62	67.93
15	45	50.27	66.96	71.28

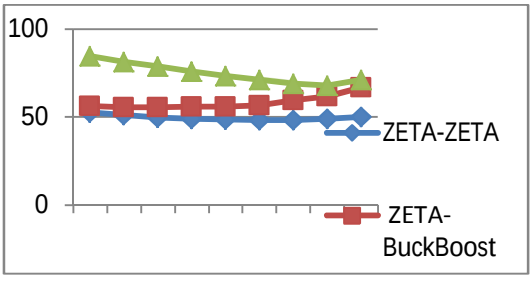


Fig 15: Plot of efficiency with D1

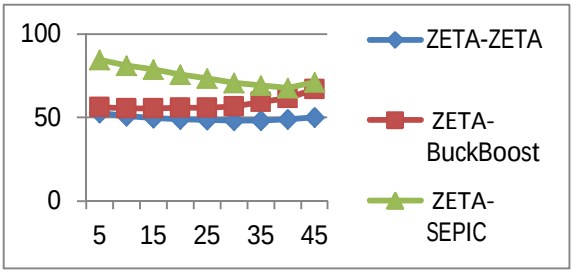


Fig 15: Plot of efficiency with D2

Simulation Results of Di Dc-Dc converters

The converter topologies are simulated in MatLab/Simulink with two different input voltages are supplied to the load through LC filter. The output voltage at the load is maintained constant by varying duty ratio. And efficiency is plotted against the operating duty cycle of the The important parameters of DI DC-DC converters like efficiency, output voltage and ripple in output current are tabulated as given in Table 7.

Table 6: Results of Simulation of DI-DC-DC Converters

SL NO	Converters type	Efficiency (%)	D1 in %	D2 in %	Output Voltage	Ripple Current
1	Buck-Buck	79.34	69	65	36	0.12
2	Buck-Buck and Boost	57.29	41	36	36	1.1
3	Buck-C'uk	78.7	52	42	36	0.33
4	Buck-SEPIC	78.39	50	41	36	0.12
5	Buck-Zeta	60.07	45	40	36	1.6
6	Boost-Boost	39.53	14	9	36	4.6
7	Boost-BuckBoost	39.46	14	9	-36	4.4
8	Boost-SEPIC	39.52	14	9	36	4.5
9	BuckBoost-BuckBoost	67.06	51	41	-36	7.7
10	BuckBoost-SEPIC	66.89	51	41	36	7.8
11	C'uk-C'uk	92.04	45	34	-36	0.2
12	C'uk-Buckboost	72.86	39	27	-36	0.9
13	C'uk-SEPIC	91.76	40	35	36	1.1
14	C'uk-Zeta	90.76	45	36	36	0.045
15	SEPIC-SEPIC	92.71	51	46	36	0.032
16	Zeta-Zeta	55.18	45	34	36	0.169
17	Zeta-BuckBoost	63.36	38	28	36	0.8
18	Zeta-SEPIC	90.08	39	33	36	1

Conclusion

In this paper the a study is carried out for the feasible topologies of DIC. An attempt is made to compare different DIC with two different input voltage sources fed to the constant load. The output voltage at the load is maintained constant by adjusting the duty cycle of both converters. The parameters like efficiency, output voltage ripple, output current ripple for the mentioned topologies are tabulated. For each of the values of the input the duty cycles are adjusted in trail and error type to maintain the output voltage constant. The changes in the operating efficiency of the converter is tabulated and plotted against duty cycle.. With this study it is possible to find the optimum duty cycle of the switches to be chosen such that efficiency is maximum. From the table and the graphs it is very clear SEPIC- SEPIC DIC is most suitable topology for hybrid power generation systems which operates at high efficiency of 89% at duty cycle of 50% also the output current ripple is also less compared to other types and is about 0.032A.

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